A Monolithic Direct-Coupled GaAs IC Amplifier with 12-GHz Bandwidth

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Abstract—A two-stage feedback amplifier with direct connection between two stages has been developed for the 0.1–12-GHz frequency band. The measured gain is 10 ± 1 dB with 2.5:1 input and 1.7:1 output VSWR. The measured minimum power output at 1-dB gain compression and maximum noise figure are 14 dBm and 9 dB, respectively, from 2 to 12 GHz. The chip size is less than 0.5×1.0 mm^2 and this area contains complete RF and bias circuitry. The amplifier also provides more than 25 dB of AGC capability.

I. Introduction

WIDE-BAND microwave amplifiers are important building blocks for modern electronic countermeasures and surveillance systems. Generally, two main circuit approaches, the traveling-wave amplifier [1], [2] and the feedback amplifier [3], [4], have been used to realize wide bandwidths from monolithic microwave integrated circuits (MMIC). For bandwidths greater than 10 GHz (two decades), both these techniques result in small gain (4–6 dB) per amplifier stage. To implement an amplifier with more than 10-dB gain over a 10-GHz bandwidth, two or more amplifier stages are required which results in a larger chip size. However, small chip size is important to ensure MMIC amplifier manufacturability with high fabrication yield and low cost.

This paper describes a two-stage feedback amplifier in which a high degree of miniaturization is achieved by using a novel direct-coupling scheme. The direct coupling of two stages eliminates the need for an interstage blocking capacitor and the associated extra bias circuitry. The complete matched amplifier is realized in a 0.5×1.0 mm^2 area resulting in an array of more than 3500 potential chips on a 2-in-diam wafer. The MMIC amplifier has 10 ± 1 dB measured gain, which is the highest gain per unit chip area reported to data for an amplifier of this bandwidth. The small amplifier size also allows packaging in conventional microwave transistor packages. The amplifier described here is a general purpose gain block which can also be used for AGC, limiting, and switching applications.

The following sections describe the circuit design, fabrication, packaging, and performance of this MMIC amplifier.

II. Circuit Design

The objective of this work was to develop a small size, low-cost, high-yield GaAs MMIC amplifier with at least 10-GHz bandwidth and 10-dB gain. Resistive feedback circuit topology was chosen to realize this objective because of its demonstrated tolerance to variations in device parameters [4]. Additionally, feedback amplifiers are well suited for monolithic realization since many device and circuit parasitics can be minimized in monolithic form. Another advantage of feedback amplifiers is their improved low-frequency stability. Feedback topology, along with direct-coupled stages, allows significant reduction in the chip area.

The basic amplifier circuit has two common-source FET stages with both series and shunt feedback. Two versions of the amplifier were realized. One version has single- and one has dual-power supply requirements. The single-power supply design, labeled *A*1, covers 2 to 12 GHz, whereas the dual-power supply design, labeled *A*2, covers 0.1 to 12 GHz and requires an external bypass capacitor.

A. DC Circuit

The circuit schematics for the two versions are shown in Fig. 1. Each amplifier stage has gate-to-drain resistive feedback which helps reduce input and output VSWR. The direct coupling of the two stages allows the drain current of the first FET to be supplied through the second-stage, feedback resistor. Thus, the drain current to both FET's is supplied through the output port. The difference between the one- and two-power supply designs is that $RS1 = 0\ \Omega$ for the two-power supply design and the dc operating point of the first stage is set by adding negative gate bias. For the dual-power supply design, the bypass capacitor C_5 is not on-chip and is added externally. The *A*2 design provides flat amplifier gain down to 100 MHz since C_5 is the main component limiting the low-frequency gain response. For both amplifier versions, the V_{DD} and V_{GG} bias is applied through external bias tees or through off-chip chokes.

The selection of dc-bias resistors is done based on the following requirements. The first FET is generally biased at 0.15–0.20 I_{DSS} to achieve a lower amplifier noise figure. This is done by proper selection of *RS*1. The second FET is generally biased at 0.50 I_{DSS} to achieve maximum power output. This is realized by proper choice of *RF*2 and *RS*2. The increase in *RS*2 and *RF*2 decreases the second FET drain current I_{DS2}. As *RS*2 increases, V_{DS2} also increases until it reaches a maximum and decreases beyond that point. This is the optimum bias point when maximum V_{DS2} is desired. The selection of *RF*2 and *RS*2 also depends on the RF circuit requirements, i.e., gain, VSWR, etc. These will be discussed later. The detailed simulation of the bias

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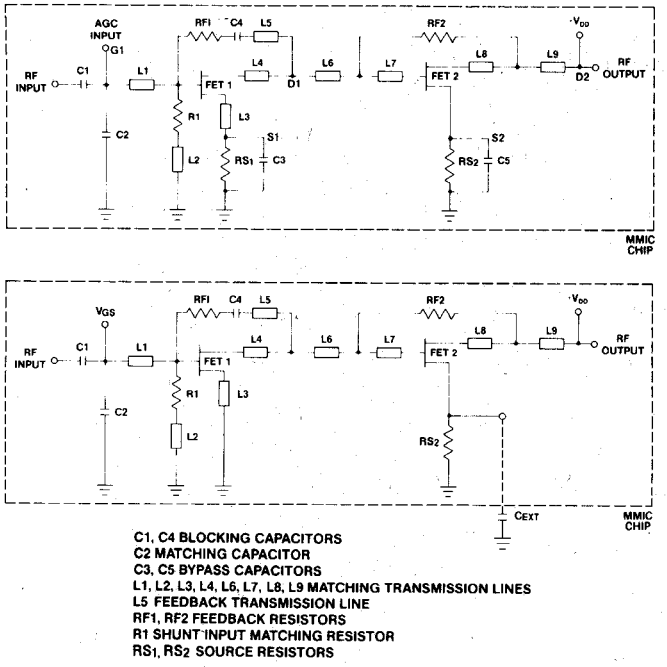

Fig. 1. Schematic of (a) single-power supply and (b) dual-power supply two-stage amplifier.

circuit was done using the SPICE JFET model. In these designs, the typical power supply requirements are +8 V and 55 mA for the one-supply design, and +8 V, −1.2 V, and 55 mA for the two-supply design.

Another advantage of this direct-coupling scheme is a decreased sensitivity of amplifier gain to variations in FET parameters. This invariance is due to the fact that changes in device I_{DSS} cause a change in I_{DS1}. However, since an increase in I_{DS1} causes a decrease in I_{DS2}, the net change in the amplifier gain due to a change in the FET bias point is small.

There are also a number of disadvantages of this biasing scheme. One limitation is that the first FET gatewidth cannot be too large, since that would result in higher I_{DS1} and consequently a large voltage drop across $RF2$. This requires V_{DD} to be very high. In this design with both FET's being 500 μm wide and with a V_{DD} of 8 V, the low I_{DS1} requirement is not a serious problem. Another limitation is the reduced amplifier RF power output capability. The amplifier RF power output cannot be increased without increasing the power dissipation in resistors $RS2$ and $RF2$. Therefore, this technique is not suited for high-efficiency applications. Additionally, the bias changes in the first FET due to gain compression adversely affect the gain compression characteristics of the second FET, resulting in an overall lower power output at 1-dB gain compression. In some cases, if the positive supply voltage is not large enough, the power output may be limited by the V_{DS} of the first FET. In this regard, the two-power supply design has slightly better power output capability since it allows higher V_{DS1}.

B. RF Circuit

The requirements for the RF circuit of this amplifier are similar to those in conventional feedback amplifiers with the exception that the dc-bias requirement, as discussed earlier, imposed a limitation on the range of FET gatewidth and feedback resistor $RF2$. For RF circuit analysis, an in-house computer analysis and optimization program (AMCAP) was used extensively in this design.

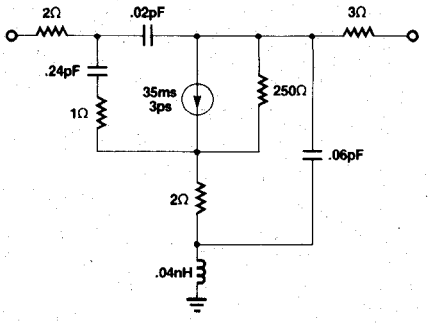

Fig. 2. A single-gate GaAs FET model for a 250-μm gatewidth device.

The equivalent circuit model of the FET was determined from S-parameter measurements taken on a number of 250-μm gatewidth devices from several wafers. Fig. 2 shows the average model parameter values for an FET biased at $I_{DS} = 0.2$ to 0.4 I_{DSS}. For a device with different gatewidths, these model values are scaled accordingly.

To optimize the performance of a high-frequency feedback amplifier, proper selection of the FET parameters is important. A number of papers have provided detailed analyses of GaAs FET feedback amplifiers [5]–[7]. To realize high forward gain, large FET transconductance is required. This implies large FET gatewidth for a given doping and gate length. Large FET gatewidth, however, is accompanied by larger Cgs and Cgd which tend to degrade the open loop gain at higher frequencies. Thus, there is an optimum gatewidth for a given gain, bandwidth, and VSWR.

The shunt feedback resistors $RF1$ and $RF2$ determine the maximum available gain and VSWR. If the feedback resistor is too large (small amount of feedback), the VSWR is generally poor. If the feedback resistor is too small, the amplifier gain is reduced [7]. In high-frequency amplifiers, the gain per stage is not very large. It is, therefore, important to realize the maximum possible gain with acceptable values of VSWR. Thus, there is an optimum value of $RF1$ and $RF2$ determined by the gain and VSWR requirements.

Based on the above discussion, the two FET's were chosen to have 500-μm gatewidth, which is close to optimum for 12-GHz operation [8]. This choice of FET's also agrees with the dc-bias requirement of low I_{DS1} for the direct-coupling scheme. In practice, this direct-coupling scheme is not ideal for feedback amplifiers below 2 GHz, due to the large FET gatewidth required [6]. $RF2$ was chosen to be 250 Ω to meet the low-output VSWR and high-gain requirements. A 2:1 output VSWR is realized easily without any additional matching elements. A low-input VSWR is difficult to achieve with feedback only. However, combined with a shunt $R-L$ network and a low-pass input matching network, the amplifier can achieve an input VSWR of better than 2:1. Without the input shunt $R-L$ network, the input VSWR at 6 GHz would be

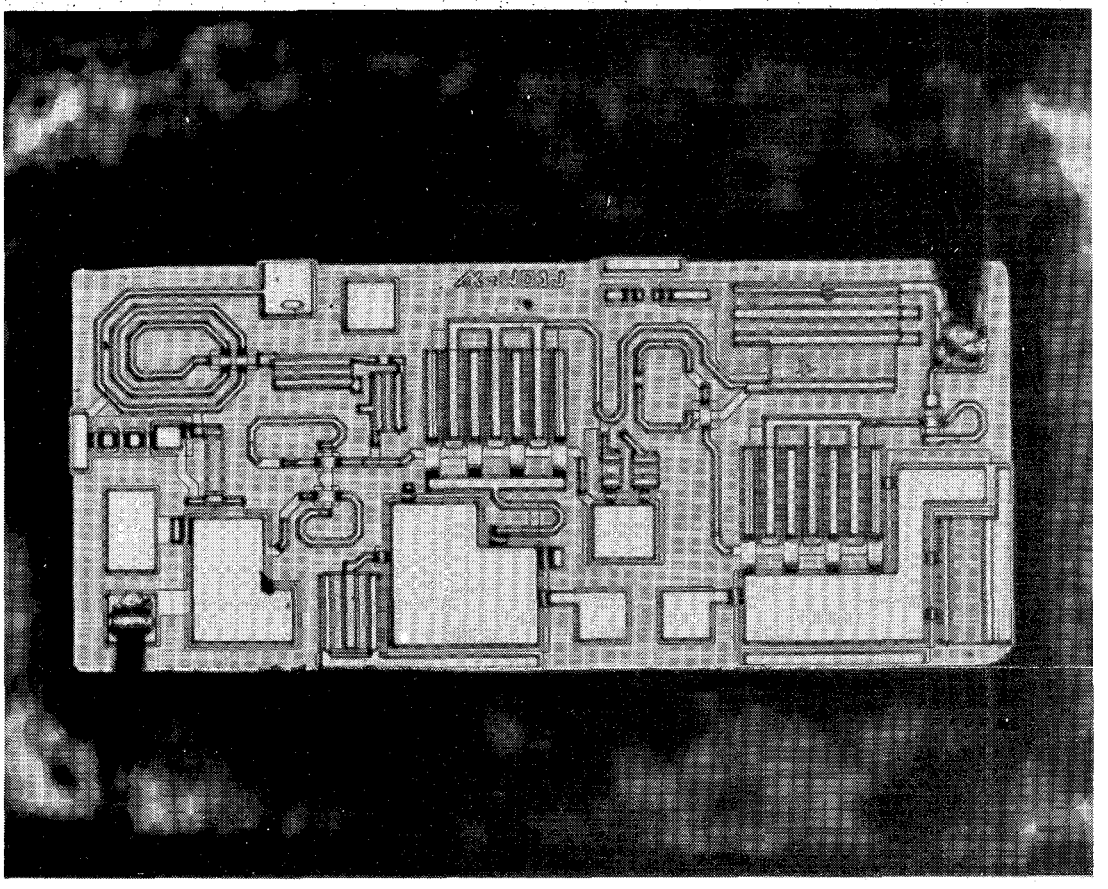

Fig. 3. A SEM photograph of the amplifier chip.

unacceptable ($> 2:1$). This frequency-dependent loss reduces the gain at 12-GHz only slightly (1 dB), but improves the VSWR at low frequencies significantly. The interstage matching network was optimized for maximum gain at 12 GHz. Overall gain of 10 ± 1 dB is obtained across 2 to 12 GHz.

An important feature of this circuit is its unconditional stability at all frequencies. This is the result of shunt and series feedback resistors which degrade the low-frequency gain significantly. No oscillations are observed, even if the input and output ports are not terminated with 50-Ω loads. This is important during wafer-level dc testing and screening of these IC's.

The RF circuit for the one- and the two-power supply designs are almost identical. The wider bandwidth of 0.1 to 12 GHz with 10 ± 1 dB gain is realized in the two-power supply design by bonding in an external capacitor C_5 of 50 pF. The bond wire inductance should be small to minimize gain degradation at 12 GHz. The power output performance of the two-power supply design is expected to be higher than the single-supply design due to higher V_{DS1}. The two-power supply design has the same chip area as the single-supply design, although it could be made smaller due to absence of on-chip bypass capacitors.

Fig. 3 shows the layout of the two-stage MMIC amplifier $A1$. The wraparound grounding technique allows easy access to RF ground on all four sides of the chip, minimizing the inductance to ground and the area used for grounding.

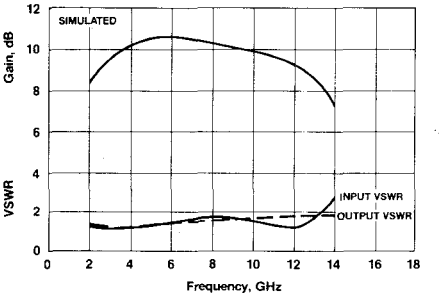

Fig. 4. Simulated gain and VSWR of the amplifier.

This chip has four different ground paths. In spite of the compact layout, care was taken to avoid coupling between certain critical circuit components and modes. Use of spiral inductors helped reduce the chip size. Inductors were modeled as high-impedance transmission lines that were fit to measurements taken on discrete inductors. [4].

Fig. 4 shows the computer-simulated results for the gain and VSWR of the MMIC amplifier. The gain at 2 GHz is limited mainly by the size of the source bypass capacitors ($C3$ and $C5$, being about 6 pF each). A larger source-capacitance value raises the gain at 2 GHz. Higher gain amplifier blocks are realized by directly cascading the chips. An input blocking capacitor of 4 pF is included for this purpose. This MMIC amplifier can also be used for AGC, limiting, and switching applications. By applying a

negative voltage to the input of the amplifier, AGC operation with 25 dB of gain control is obtained.

III. Fabrication

Ion-implanted GaAs is used as the starting material for the IC's due to its excellent uniformity and controllability. After implantation, the wafers are annealed at 800 °C upon which the sheet resistance drops to approximately 500 Ω/square. This layer is then selectively etched to form mesas for the FET's and resistors. Later, the resistor mesas are etched to trim the sheet resistance to 800 Ω/square. In practice, this technique yields standard deviations in resistance of less than 15 percent.

The FET's in the IC are fabricated with the same process used for discrete FET's. The gates are formed on a nominally 0.5-μm-long base of TiW/Au which is gold plated to 0.7 μm. The resulting structure combines very short gate-length with large gate cross-sectional area for high device transconductance with low parasitics [9]. Source and drain ohmic contacts are formed with an AuGe/Ni alloy. Parallel-plate dielectric capacitors are fabricated with plasma-enhanced CVD silicon nitride and provide 390 pF/mm^2 of area. This procedure is also well controlled and achieves standard deviations of less than 40 pF/mm^2.

Metallic interconnections are achieved with a two-level wiring process which provides surface connections, crossovers, and air bridges. The top level is situated 3 μm above the GaAs surface and gold plated to 1.5 μm. The bottom level rests directly on a semi-insulting GaAs substrate and is 0.8 μm thick. These lines are normally designed for a current density not to exceed 5×10^5 amps/cm^2.

Wraparound ground technology is chosen over via-hole ground technology for low parasitic inductance and improved area efficiency. To form the wraparound, metal is first deposited and gold plated to 2 μm on the frontside of the chips. The wafer is then lapped to 115 μm and backside metallized to complete the wraparound ground connection.

IV. Measured Results

All the results presented in this section are for the single-power supply design, except when specified otherwise. The dual-power supply results are presented for wider bandwidth and higher power output.

A. DC Characteristics

Functional dice are selected by extensive automated dc wafer probing followed by visual inspection. Defective dice are indentified by measuring the drain current, transconductance, and pinchoff voltage of the individual transistors, as well as the values of the resistors (except the resistor *RF*1). Fig. 5 shows a histogram of the FET pinchoff voltage distribution. The average V_p and standard deviation for FET1 are −1.98 and 0.21 V, respectively. These values are similar to those reported previously [10]. This high degree of uniformity is due to the use of ion-implanted GaAs substrates. FET uniformity is very important in realizing high amplifier RF yield.

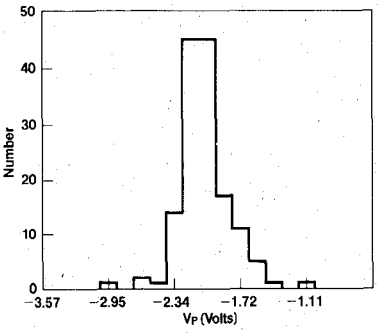

Fig. 5. Histogram showing V_p distribution of ion-implanted FET's.

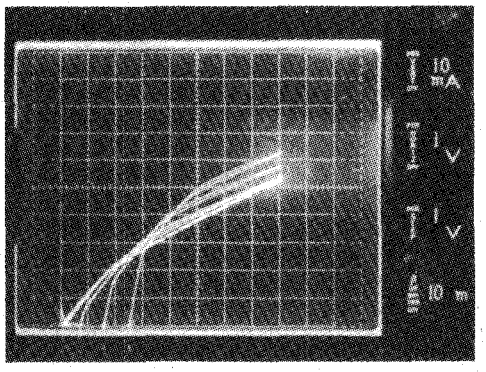

Fig. 6. Two-stage MMIC amplifier I/V characteristics.

The dc functional dice are then mounted on a metallized alumina test carriers which are via-hole grounded at the center and have 50-Ω input and output microstrip lines on each side. When the power supply is ramped from 0 to V_{DD}, a properly biased amplifier will exhibit the dc $I-V$ characteristic shown in Fig. 6.

For $V_{GG}=0$ V, the dc supply current increases from zero at a rate of about 10 mA/V until the dc voltage supply approaches +2.0 V. Above 2.0 V, the dc current increases at about 5 mA/V due to the initiation of self-biasing of the second FET.

This two-section $I-V$ curve is the characteristic signature of a properly biased amplifier. The normal dc operating bias is +8V and 55 mA. Fig. 5 also shows the $I-V$ curves for negative V_{GG}.

B. Amplifier Performance

Fig. 7 shows the measured gain and VSWR of the MMIC amplifier. The measurements are in good agreement with the simulated results showing 10±1-dB gain across the 2–12-GHz band. The gain flatness can be improved by using larger bypass capacitors *C*3 and *C*5. The maximum input VSWR is 2.5:1 across the band. This is slightly higher than the design goal of 2:1. This discrepancy is due to the FET *Cgs* being actually smaller than the modeled value. The output VSWR is better than 1.7:1 across the band.

The noise-figure performance of the amplifier is shown in Fig. 8. The noise-figure modeling was performed using an empirical FET noise model reported previously [11]. The measured noise figure is typically 6 dB with a maxi-

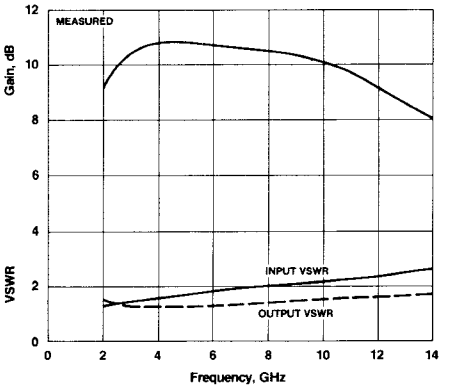

Fig. 7. Measured gain and VSWR of the amplifier.

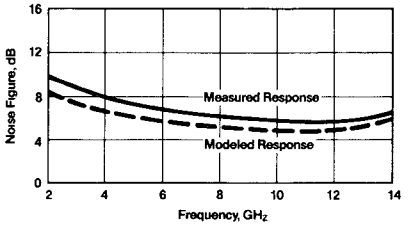

Fig. 8. Measured and modeled noise figure of the amplifier chip.

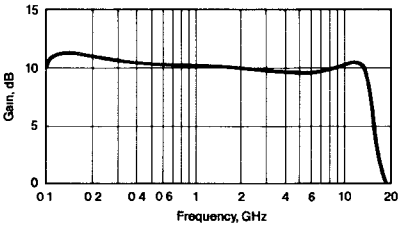

Fig 9. Measured gain of 0.1 to 12-GHz amplifier.

mum of 9 dB at 2 GHz. The measured noise figure is slightly higher than the modeled noise figure. This may be due to line loss in the input and interstage transmission lines being higher than originally modeled. The noise figure at 2 GHz is higher than that at 12 GHz due to extra loss in the input shunt $R-L$ network ($R1$ in Fig. 1) at lower frequencies.

Fig. 9 shows the measured gain of the $A2$ amplifier with a 50-pF external bypass capacitor. Gain of 10 ± 1 dB is obtained across the 0.1 to 12-GHz band. Four bond wires are used to minimize the source inductance from FET2 to the external capacitor. Still, this inductance degrades the gain by about 0.4 dB at 12 GHz. The VSWR for this amplifier is similar to that of Fig. 6 since the VSWR across 0.1 to 2-GHz band is always better than 1.7:1.

A plot of the output power versus input power of the $A1$ amplifier is shown in Fig. 10. At the nominal bias voltage of +8V, a saturated power output of +13 dBm is obtained across the band. At +12 V, a saturated power output of 15 dBm is obtained. Fig. 11 shows a plot of power output at 1 dB gain compression, P_{-1} versus frequency for $A1$ and $A2$ amplifiers. For the $A1$ amplifier, a minimum P_{-1} of 11 dBm is obtained. P_{-1} is less at 8 GHz than at 12 GHz, indicating that the output and the interstage match is not optimized for the best amplifier large-signal performance.

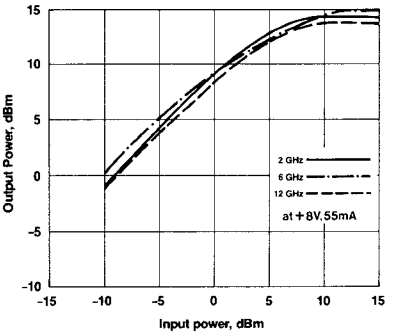

Fig. 10. P_{out} versus P_{in} of the amplifier.

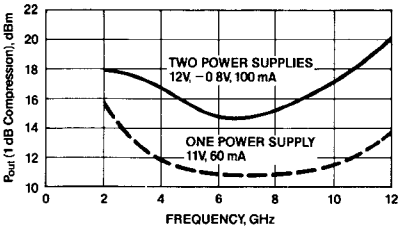

Fig. 11. P_{-1} versus frequency of the amplifier.

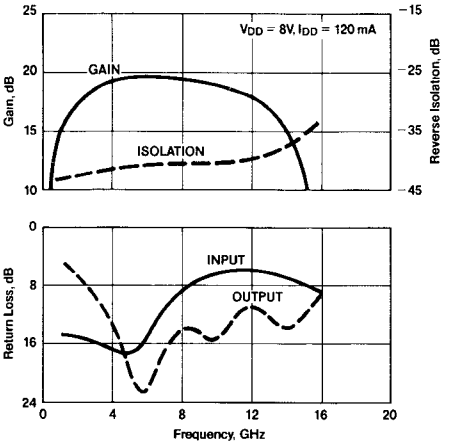

Fig. 12. Gain and return loss of two MMIC chips cascaded directly.

The bias for the FET's were optimized for maximum power output by adjusting $RS1$ and $RS2$ with external resistors. To prevent FET1 from going into the nonlinear region, the I_{DS1} and V_{DS1} should be large. This requires a larger voltage drop across $RF2$ and therefore larger V_{DD}. The $A2$ amplifiers have larger V_{DS1} for a fixed V_{DD} since $RS1 = 0\ \Omega$. This is part of the reason why P_{-1} for the $A2$ is higher than that for the $A1$ amplifier. Another reason is that, for the same V_{DS1} and I_{DS1}, V_{D1} is lower on the $A2$ amplifier. This allows I_{DS2} to be adjusted to about 0.5 I_{DSS} rather than close to I_{DSS}. Thus, the dual-power supply design has the two main advantages of wider bandwidth and higher power output.

Higher gain amplifiers were realized by directly cascading two MMIC chips. Fig. 12 shows the performance of

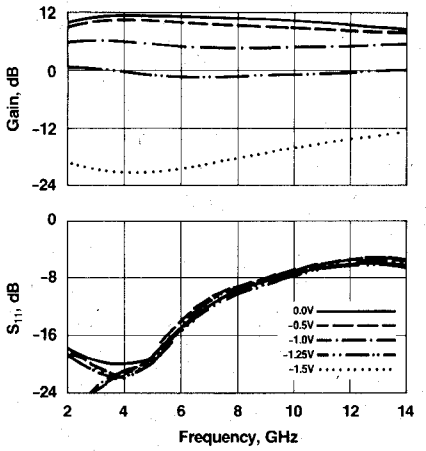

Fig. 13. AGC response of the amplifier.

this four-stage amplifier (two chips). A gain of 18 ± 1.5 dB is obtained across the 2–12-GHz band, indicating that the gain flatness does not degrade significantly. Input and output return loss are better than 6 and 8 dB, respectively.

Since the MMIC chip is less than 0.5×1.0 mm^2, it can fit easily into a variety of microwave transistor packages. These include the standard 70-mil flange, 70-mil stripline, and 100-mil flange package. The amplifier VSWR and gain flatness degrades slightly if the package leads do not have 50-Ω characteristic impedances. With improved gain flatness and VSWR, this is not expected to be a problem. The appropriate package for a given application is determined by the cost, hermeticity, and heat dissipation requirements. The amplifier performance was also tested over temperature. The gain decreases typically at the rate of 0.02 dB/°C over the temperature range of −55° to 75°C.

C. AGC Switching and Limiting Applications

The AGC operation of the MMIC amplifier is realized by applying either positive or negative voltage to the gate of the first FET. With positive V_{GG}, I_{DS1} increases causing a decrease in V_{DS1}. As V_{DS1} drops below 1.5 V, the amplifier gain starts to drop significantly. When negative V_{GG} is applied, the g_m of the first FET drops, causing a reduction in the amplifier gain. Of the two techniques, applying negative V_{GG} maintains better gain flatness across the 2–12-GHz band. With positive V_{GG}, the AGC response shows steeper slope with less gain decrease at higher frequencies. Fig. 13 shows the AGC performance of the amplifier. More than 25 dB of gain variation is realized without affecting the input VSWR significantly.

As a limiting amplifier, power output of up to 15 dBm can be realized. For lower power output, AGC response with positive or negative V_{GG} can be used, in which case the power output is limited by the first FET.

A broad-band single-pole single throw switch is realized by applying large (> 2 V) negative V_{GG}. About 30 dB of on/off ratio can be obtained. For even greater (more than 40 dB) on/off ratios, V_{DD} can be turned off to 0 V. Even in this case, the input VSWR does not change significantly.

V. Conclusions

Design and performance of a two-stage, resistive feedback, direct-coupled amplifier is described. This amplifier provides 10 ± 1-dB gain across the 0.1 to 12-GHz band. The size of this MMIC amplifier chip is reduced to below 0.5×1.0 mm^2 by utilizing a novel direct-coupled interstage bias scheme. The resulting large number of die per wafer reduce the per-chip cost. The chip amplifier also provides AGC, switching, and limiting operation and allows multistage cascading and is compatible with conventional microwave transistor packaging.

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References

[1] Y. Ayasli, R. L. Mozzi, J. L. Vorhaus, L. D. Reynolds, and R. A. Pucel, "A monolithic GaAs 1–13 GHz travelling-wave amplifier," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-30, pp. 976–981, July 1982.

[2] E. W. Strid and K. R. Gleason, "A dc-12 GHz monolithic GaAs FET distributed amplifier," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-30, pp. 969–975, July 1982.

[3] D. P. Hornbuckle and R. L. Van Tuyl, "Monolithic GaAs direct-coupled amplifiers," *IEEE Trans. Electron Devices*, vol. ED-28, pp. 175–182, Feb. 1981.

[4] S. Moghe, T. Andrade, G. Policky, and C. Huang, "A wideband two stage miniature amplifier," *IEEE 1983 GaAs IC Symp. Dig. Papers*, pp. 7–10.

[5] K. B. Niclas, W. T. Wilser, R. B. Gold, and W. R. Hitchens, "Matched feedback amplifier—Ultrawide-band microwave amplification with GaAs MESFET's," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-28, pp. 285–294, Apr. 1980.

[6] W. C. Petersen, A. Gupta, and D. R. Decker, "A monolithic GaAs dc to 2 GHz feedback amplifier," *IEEE Trans. Electron Devices*, vol. ED-30, pp. 27–29, Jan. 1983.

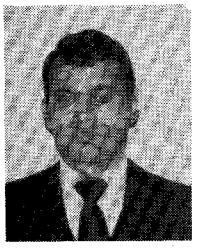
[7] A. M. Pavio and S. D. McCarter, "Network theory and modeling method aids design of a 6–18 GHz monolithic multi-stage feedback amplifier," *Microwave Syst. News*, pp. 78–93, Dec. 1982.

[8] P. N. Rigby, J. R. Suffolk, and R. S. Pengelly, "Broadband monolithic low noise feedback amplifiers," in *IEEE 1983 Microwave and Millimeter-wave Monolithic Circuits Symp. Dig. Papers*, pp. 71–75.

[9] C. Huang, A. Herbig, and R. Anderson, "Sub-half micron GaAs FET's for applications through *K*-band," in *IEEE 1981 Microwave Symp. Dig. Papers*, pp. 25–27.

[10] T. Sugiura, H. Itah, T. Tsuji, and K. Honjo, "12 GHz band low noise GaAs monolithic amplifiers," *IEEE Trans. Electron Devices*, vol. ED-30, pp. 1861–1866, Dec. 1983.

[11] P. W. Chye and C. Huang, "Quarter-micron low noise FET's," *IEEE Electron Dev. Lett.*, vol. EDL-3, pp. 401–403, Dec. 1983.



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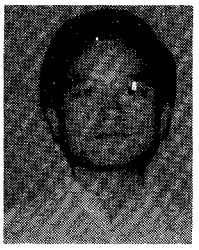

Horng-Jye Sun was born in Sze Chuan, China, on August 10, 1949. He received the B.S.E.E. and M.S.E.E. degrees from the National Taiwan University, Taipei, Taiwan, in 1971 and 1975, respectively, and the Ph.D. degree from Reneselaer Polytechnic Institute, Troy, NY, in 1982.

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Thomas Andrade (M'80) photograph and biography not available at time of publication.

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Dr. Huang is a member of Eta Kappa Nu.

Capacitively Coupled Traveling-Wave Power Amplifier

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Abstract—**A new circuit concept which significantly improves the power-handling capability of a traveling-wave amplifier by coupling the active devices to the input gate line through discrete series capacitors is described. The approach is applied to a 1-W, 2–8-GHz monolithic amplifier design.**

I. Introduction

DISTRIBUTED or traveling-wave amplifiers covering wide microwave bands have been reported in recent years [1]–[5].

Designing a traveling-wave amplifier for maximum power, however, requires several additional considerations [6]. One is the limitation of input power. With a 50-Ω gate line and pinchoff voltages on the order of −4 V, the maximum power input is about 50 mW. A design allowing an increase in power input without sacrificing gain must be utilized.

In this paper, we present a circuit concept which significantly improves the power-handling capability of a traveling-wave amplifier by coupling the active devices to the input gate line through discrete series capacitors. Combined with the gate–source capacitance of the FET's, these capacitors act as voltage dividers, allowing us to sample a desired portion of the input signal from the gate line. In addition, by varying the divider ratio along the gate line, it is possible to tailor the input excitation to individual FET's. In this manner, the input power can be increased significantly (typically by a factor of four) and the total device periphery can be at least doubled. This should result in increased power output and efficiency.

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